Top Gate Amorphous In−Ga−Zn−O Thin Film Transistors Fabricated on Soda−Lime−Silica Glass Substrates

Gwanghyeon Baek*, Alex Krasnov**, Willem den Boer**, Jerzy Kanicki*

* Electrical Engineering and Computer Science, University of Michigan, Ann Arbor, MI, United States
** Guardian Industries Corporation Science and Technology Center, Carleton, MI, United States

Abstract

This work presents a comparative analysis of top gate a-IGZO TFTs fabricated on both soda-lime-silica glass and alkali-free borosilicate glass. Low-temperature ALD is selected for the deposition of gate dielectric to minimize a thermal stress. Comparing with TFTs on alkali-free borosilicate glass, TFTs with soda-lime-glass show similar threshold voltage and sub-threshold swing, but slightly degraded effective mobility, stability and uniformity. The results of atomic force measurements are provided to explain the uniformity degradation.

Author Keywords

soda−lime; soda−lime−silica; borosilicate; glass; substrate; thin-film transistor; TFT; a-IGZO; stability; uniformity

1. Introduction

Today glass substrates for thin-film transistors' (TFTs') array have been made of alkali-free borosilicate glass. The non-alkali borosilicate glass has high thermal and dimensional stability, which are critical in enabling a glass substrate to withstand the multiple elevated temperature processing steps required of deposition and etch processes and to ensure precision registration during lithography process of different layers. [1] In addition, this type of glass substrates minimizes alkali-ion diffusion from glass to thin films which could degrade TFT's performance and electrical reliability. However, due to its special manufacturing process, it is known that the borosilicate glass is more expensive than regular glass, such as window glass, which is made of soda-lime-silicate. (a.k.a soda-lime glass) In view of lowering cost of the flat panel displays, the use of the alkali-free borosilicate glass as a substrate for amorphous-silicon (a-Si) and/or poly-silicon TFTs' array need to be reconsidered.

Recently, the amorphous In-Ga-Zn-O (a-IGZO) TFTs have received considerable attention as a possible replacement of a-Si TFTs. [2] The most attractive features of a-IGZO TFTs are the high electron mobility (μ_{eff}) in amorphous state, which can be achieved at low-temperature processing. This leads a doubt about the necessity of the use of borosilicate glass for a-IGZO TFT's substrate. Despite numerous results on a-IGZO TFT itself have been reported, there is a lack of information on glass effect, particularly, on compatibility of soda-lime (SL) glass with a-IGZO TFTs. At the same time, the SL glass has successfully made its way into the photo-voltaic semiconductors use. [1, 3] In this regard, it would be beneficial to investigate in detail the SL glass as a-IGZO TFTs' substrate.

This work presents a comparative analysis of top gate a-IGZO TFTs fabricated on both soda-lime glass and alkali-free borosilicate glass. The electrical performance, stability and the performance uniformity of TFTs fabricated on different glass substrates are discussed.

2. Experimental

The a-IGZO TFTs used in this study have the staggered structure (top gate structure). The cross-sectional view of the fabricated TFTs is illustrated in Figure 1. The TFTs are fabricated on four different substrates;

1. **Reference:** commercial TFT-grade glass substrate which is made of alkali-free borosilicate

2. Bare soda-lime glass **(SL)** without barrier layer

3. Soda-lime with barrier layer of Boron-doped SiO_x **(SiBOx)**

4. Soda-lime with barrier layer of Silicon Oxy-Nitride **(SiON)**

Soda-lime glass, 0.7mm thick, had a typical composition of a regular float. Both SiBOx and SiON layers had a thickness of 80 nm and near-stoichiometric composition. SiON is a traditionally used material for preventing the migration of alkaline elements, such as Na, Ca, K, etc. Its barrier properties, however, depend strongly on the presence of aluminum, which is used in the target material (silicon) to facilitate dc sputtering. Si targets in this research had an aluminum concentration of 8 wt%. Aluminum is known to affect the length of the Si-O bond, thus compromising the barrier properties of the SiON. Fabrication of
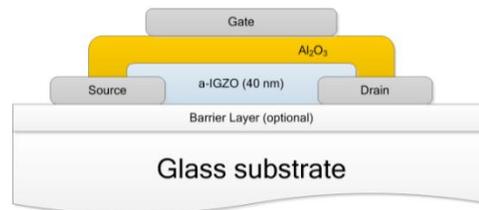
Figure 1. Cross-sectional structure of the fabricated a-IGZO TFTs. Low-temperature atomic layer deposition (LT-ALD) is used for the gate dielectric.

| (a) | (b) |
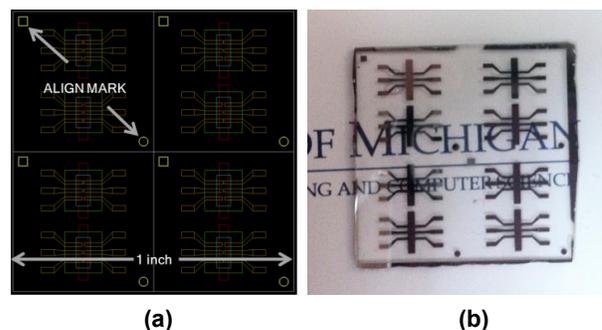
Figure 2. (a) Mask layout used in this work. (stencil mask) and **(b)** picture of fabricated TFTs on soda-lime (SL) glass substrate. Substrates have a shape of square with side length = 1 inch.
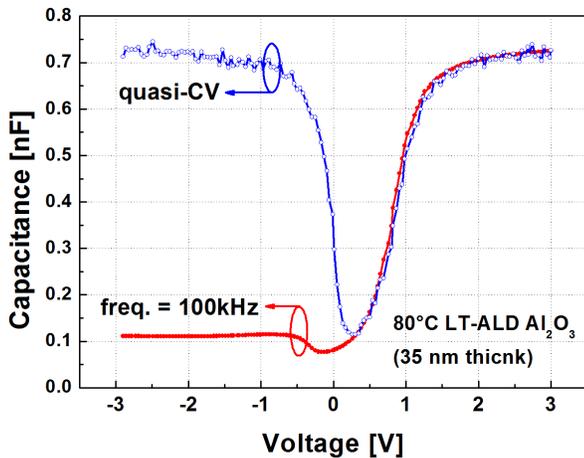
Figure 3. Capacitance-Voltage curves of MOS capacitor with Al_2O_3 dielectric. Al_2O_3 dielectric is deposited by low temperature atomic layer deposition (LT-ALD), 80 °C.
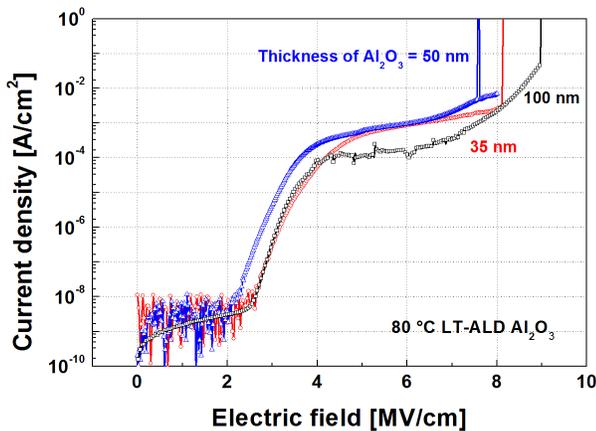
Figure 4. The breakdown voltages of LT-ALD Al_2O_3 with three different thickness are demonstrated. The breakdown voltage of the fabricated dielectric is > 7 MV/cm.

Al-free sputtering targets is an ongoing development. To explore the use of an alternative barrier, SiBOx was used. SiBOx is known for its superior sodium-blocking properties with some concerns, however, regarding the stability of boron in it. The concentration of B in Si targets in this experiment was 2 wt%.

As a first step, the substrates were cleaned with acetone, IPA and D.I. water. After drying the cleaned substrate at 105°C for 1 min., the Mo layer (40 nm) was sputtered on the substrate as the source/drain electrodes at room temperature (R.T.). The a-IGZO channel layer (45 nm) was deposited by sputtering at R.T. (No intentional heating is applied) The a-IGZO sputtering target consists of In:Ga:Zn:O with molar ratio of 1:1:1:4. The used sputtering power and pressure were 300W (R.F) and 3 mTorr, respectively. The sputtering target had a diameter of 3 inch and the distance between the sputtering target to the substrate was about 8 inch. The sputtering chamber ambient was maintained with a mixture of Ar and O_2 (Ar=50 sccm, O_2=1 sccm).

SL substrate is 2.6 times less resistant to thermal expansion than borosilicate glass. The linear thermal expansion coefficients of SL and borosilicate glass are 8.6×10^{-6} and 3.3×10^{-6} per 1 °C, respectively. [4,5] This implies that the SL is required to have 2.6 times reduced process temperature from regular borosilicate glass to maintain the same level of thermal expansion. The gate

dielectric of a-IGZO TFTs is typically deposited by PECVD with a temperature range of $300 \sim 400$ °C. [2]

In this experiment, the low temperature (80 °C) atomic layer deposition (LT-ALD) was used to deposit Al_2O_3 gate dielectric. We believe that LT-ALD is able to deposit a high quality gate dielectric with minimizing the thermal stress on SL glass. The tri-methyl-aluminum (TMA) and water were sequentially injected into the deposition chamber. The Al_2O_3 dielectric was acting not only as a gate dielectric, but also as a passivation layer in the top gate structure. The deposition of the gate dielectric was followed by sputtering of a gate electrode, 80−nm−thick Mo. Finally the TFTs underwent a thermal annealing step at 250 °C in atmosphere at the end of the device processing for 30 minutes. The channel width/length (W/L) is 300 μm / 50 μm. A sufficient overlap between top and bottom gate electrodes was used in the TFT layout to avoid misalignment. All substrates are fabricated at the same time to avoid a process variation. The mask layout and picture of the fabricated device are shown in Figure 2.

In order to confirm the quality of LT-ALD Al_2O_3 and estimate a dielectric's permittivity, we measured the capacitance-voltage (C-V) characteristics of Al_2O_3 layer using MOS-capacitor structure. The extracted permittivity is 6.5 ε_0, where ε_0 is the permittivity of the air. The flat-band voltage and break down voltage is 0.2 V and > 7 MV/cm, respectively. (Figure 3 and 4) From these results, we conclude that the LT-ALD Al_2O_3 is suitable for TFT applications.

3. Result and Discussion

The TFTs' electrical properties are measured by Agilent B1500A semiconductor device parameter analyzer. Figure 5 and 6 illustrate the linear region (V_{DS} = 0.5 V) transfer characteristics of various substrates. The V_{TH}, μ_{eff} and SS are extracted to be -2.7 V, 13.6 cm^2/V-sec and 400 mV/dec, respectively, for TFT on the glass reference. The soda-lime glass TFTs also have a similar V_{TH} and SS, however μ_{eff} is degraded from the glass reference by about 35%. V_{TH} for SL glass seems to be slightly more negative in comparison to reference glass. We could speculate that small quantities of positive ions such as Na+ are diffusing from the glass into a-IGZO layer during TFT fabrication. Table 1 summarizes all the TFT key parameters.
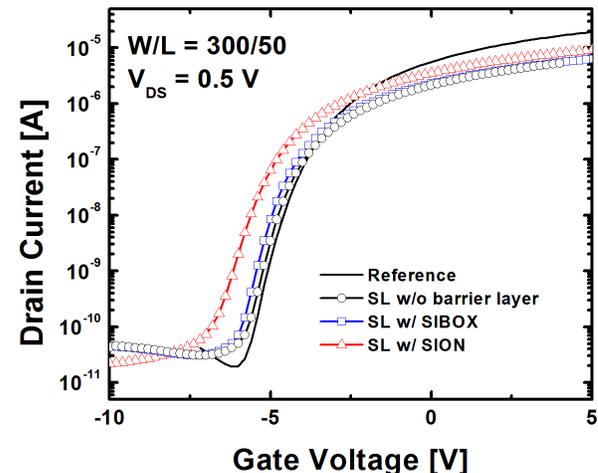
Figure 5. Transfer characteristics of a-IGZO TFTs, which are fabricated on four different glass substrates. Various substrates are labeled.
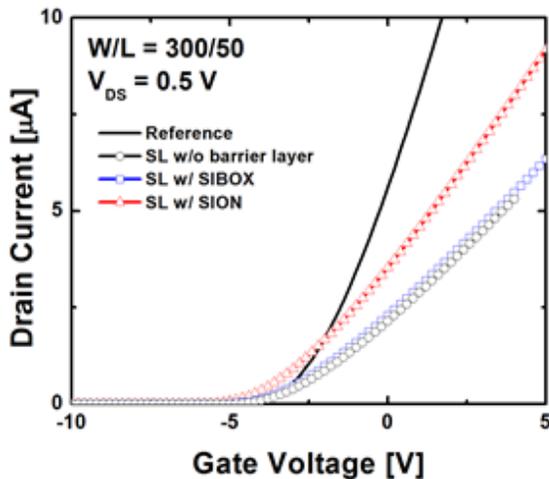
Figure 6. Transfer characteristics of the fabricated a-IGZO TFTs in linear scale.

Figure 7. Negative bias temperature stability (NBTS): TFT threshold voltage shift (ΔV_{TH}) as a function of stress time. V_{STR} = -15 V is applied on TFT's gate with T_{STR} = 80 °C, V_{DS} = 0 V.

The TFT parameter extractions are based on the standard MOSFET equations and are discussed in more detail in [6]. The hysteresis voltage, V_{TH} difference from forward and reverse gate sweep, for all TFTs are smaller than 0.1 V.

Next, the bias-instabilities of each TFT are investigated. For the negative bias-temperature-stress (NBTS), the stress voltage, V_{STR} = -15 V, is applied on the gate electrode for certain stress time and the drain terminal is shorted to source terminal (V_{DS} = 0 V). The stress temperature (T_{STR}) is fixed at 80 °C. The evolutions of V_{TH} (ΔV_{TH}) as a function of stress-time are summarized in Figure 7. The best linear fitting method for 10% to 90% of the maximum drain current is used for the V_{TH} extraction.[6] The changes in sub-threshold swing and field effect mobility are negligible. The TFTs with soda-lime glass show around -6 V shift on its V_{TH}, whereas the reference TFT shows only -1.8 V. The ΔV_{TH} of TFTs on SL glass substrate are significantly larger than that of glass reference TFTs, but still comparable with ΔV_{TH} of a-Si TFTs, which have been reported by others. (using TFT-grade glass substrate.) [7,8] It should be noticed that in all cases during NBTS we have negative shift of the threshold voltage indicating accumulation of the positive changes either within back channel or channel layer or/and near the a-IGZO / gate insulator interface. This positive charge could be very well Na+ ions present in SL glass and diffusing to a-IGZO during TFT fabrication process. Two proposed barrier-

layers are not very effective in stopping positive ions diffusion from the SL substrate. Further improvements in the barrier layer will be needed.

Lastly, we study the uniformity of the fabricated TFTs. Total six TFTs over 1 inch by 1 inch square area are measured for different glass substrates and their TFT parameters are extracted using the same method mentioned above. The standard deviation (σ) values of the extracted parameters are tabulated in Table 1. The variation on μ_{eff} and SS are similar for all substrates. However, V_{TH} variations on SL glass substrate are worse than the reference glass.

To address the worsened uniformity, the surface flatness is measured by atomic force microscopy (AFM). From Figure 8, the surfaces of SL glass are less flat comparing with the reference glass. The SL with SiBOx glass is the least flat one among four samples and also shows the worst V_{TH} uniformity. Therefore, the correlation between surface flatness and TFT's uniformity might be suspected, yet further study on this subject is required. We were wondering if not only the uniformity but also the reduced mobility and stability on soda-lime glass are caused by the increased surface roughness (as seen in Figure 8). The composition of the glass may not make a difference for

Table 1. The extracted TFT parameters (linear region where V_{DS}=0.5V) and parameters' uniformity over 1-inch × 1-inch square area. Standard deviations (σ) are calculated from six identical TFTs for each substrate.

	V_{TH} (V)	μ_{eff} (cm²/Vs)	SS (mV/dec)	σ(V_{TH}) [V]	σ(μ_{eff}) [cm²/V-sec]	σ (SS) [mV/dec]
Reference	-2.7	13.6	400	0.3	0.21	8.2
SL w/o barrier layer	-3.1	8.2	450	0.6	0.17	8.3
SL w/ SiBOx	-2.9	8.7	400	1.5	0.25	14.8
SL w/ SiON	-3.6	9.1	600	0.7	0.19	9.5
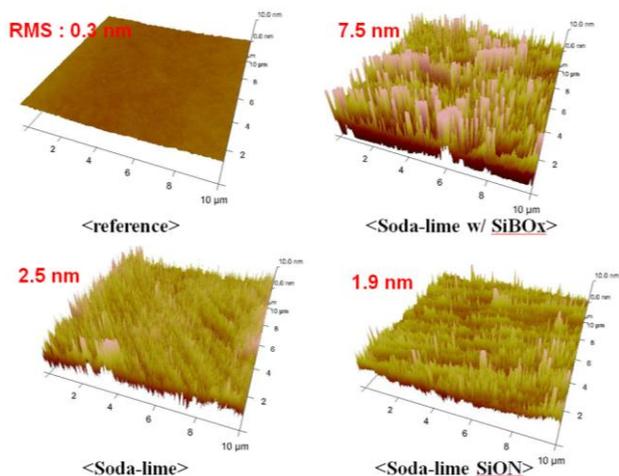
Figure 8. Surface flatness of substrates are measured by atomic force measurement. Root-mean-square (RMS) values are described in upper left side of each figure.

mobility and stability, since mobility and stability are similar or close with and without a barrier layer.

4.   Conclusion

The a-IGZO TFTs are successfully fabricated on soda-lime glass substrates and their electrical characteristics are compared with reference TFTs, which are fabricated on borosilicate (commercial TFT-grade glass) substrate. Al_2O_3 with LT-ALD (80 °C) is used to deposit a high quality gate dielectric with minimizing the thermal stress, which negatively affects SL glass. TFTs on soda-lime glass showed proper switching characteristics with V_{TH} = -3.1 V, μ_{eff} = 8.2 cm^2/V-sec, SS = 450 mV/dec and $\sigma(V_{TH})$ = 0.6 V. The values of V_{TH} and SS are similar with the reference, while bias-instability (ΔV_{TH}) and $\sigma(V_{TH})$ have degraded values. The effect of different barrier layers is not significantly observed. Further investigations of the degraded uniformity and electrical stability of TFTs on soda-lime glass, and microscopic origin responsible for threshold voltage shift are still necessary. It is also concluded from this study that the glass surface smoothness is critical in achieving uniform a-IGZO TFT electrical properties.

We are expecting the TFTs fabricated on soda-lime substrates could

1.   reduce the manufacturing cost by adapting inexpensive substrate material

2.   be utilized for the development of display applications for vehicle and architectural windows. [9]

This research represents an important step toward above applications.

6.   References

[1]   T. Kloss, G. Lautenschläger, K.T. Schneider, "Advances in the process of floating borosilicate glasses and some recent applications for specialty borosilicate float glasses" Glass Technology − European Journal of Glass Sci. and Tech. Part A, **41(6)**, Dec., 177-181 (2000)

[2]   H. Kumomi, S. Yaginuma, H. Omura, *et al.*, "Materials, Devices, and Circuits of Transparent Amorphous-Oxide Semiconductor" Journal of Display Technology, **5(12)**, 531-540 (2009)

[3]   M. Shao, A. Fischer, D. Grecu, U. Jayamaha, E. Bykov, G. Contreras-Puente, R. G. Bohn and A. D. Compaan, "Radio-frequency-magnetron-sputtered CdS/CdTe solar cells on soda-lime glass" **69(2)**, 3045-3047 (1996)

[4]   Material Information Sheet - Corning Eagle XG AMLCD Glass Substrates

[5]   W. L. Konijnendijk, J. M. Stevels "The linear expansion of borosilicate glasses in relation to their structure" Verres Réfract., **30(**3), 371, (1976)

[6]   G. Baek, K. Abe, A. Kuo, H. Kumomi, J. Kanicki, "Electrical Properties and Stability of Dual-Gate Coplanar Homojunction DC Sputtered Amorphous Indium–Gallium–Zinc–Oxide Thin-Film Transistors and Its Application to AM-OLED" Electron Devices, IEEE Transactions on, **58(12)**, 4344 – 4353, (2011)

[7]   G. Yoo, H. Lee, J. Kanicki "Electrical Stability of Hexagonal a-Si:H TFTs" Electron Device Letters, IEEE, **31(1)**, 53–55 (2010)

[8]   F. R. Libsch and J. Kanicki "Bias-stress-induced stretched-expontial time dependence of charge injection and trapping in amorphous thin-film transistors" App. Physics Let., **62**, 1286-1288 (1993)

[9]   T. Watanabe, S. Fukayama, M. Miyauchi, A. Fujishima, K. Hashimoto, "Photocatalytic Activity and Photo-Induced Wettability Conversion of TiO_2 Thin Film Prepared by Sol-Gel Process on a Soda-Lime Glass" Journal of Sol-Gel Science and Technology, **9(1-3)**, 71-76, (2000)